CLAIMS

1. A method of packaging an integrated circuit die, comprising the steps of:

providing a foil sheet;

forming a layer of solder on a first side of the foil sheet;

attaching a first side of an integrated circuit die to the solder on the foil sheet, wherein the first side of the die includes a layer of metal thereon and a second, opposing side of the die includes a plurality of bonding pads;

electrically connecting the bonding pads to the solder on the foil sheet with a plurality of wires;

encapsulating the die, the electrical connections, and the first side of the foil sheet with a mold compound; and

separating the foil sheet from the die and the plurality of wires, thereby forming a packaged integrated circuit.

2. The method of packaging an integrated circuit according to claim 1, wherein the foil sheet comprises a bare metal sheet.

3. The method of packaging an integrated circuit according to claim 2, wherein the metal sheet comprises one of copper and aluminum.

4. The method of packaging an integrated circuit according to claim 1, wherein the solder is formed on the foil sheet via a screen printing process.

5. The method of packaging an integrated circuit according to claim 4, wherein the solder layer has a thickness of about 0.1 mm.

6. The method of packaging an integrated circuit according to claim 1, further comprising performing a first reflow process after the die attach step.

7. The method of packaging an integrated circuit according to claim 6, wherein the first reflow process melts the solder, thereby securing the die to the foil sheet.

8. The method of packaging an integrated circuit according to claim 1, wherein the plurality of wires are attached to the bonding pads and the solder via a wire bonding process.

9. The method of packaging an integrated circuit according to claim 1, wherein the wirebonding process comprises a ball bonding process.

10. The method of packaging an integrated circuit according to claim 9, wherein squashed ball bonds are formed on the foil sheet, said ball bonds having a diameter of about 0.25 mm.

11. The method of packaging an integrated circuit according to claim 1, wherein the wires have a diameter of about 50 um to about 100 um.

12. The method of packaging an integrated circuit according to claim 1, wherein the foil sheet is separated from the die and the wires via a second reflow process.

13. The method of packaging an integrated circuit according to claim 1, wherein a portion of the solder remains

attached to the wires and the die after the foil sheet is separated therefrom.

14. The method of packaging an integrated circuit according to claim 1, wherein the more than one die is attached to the foil sheet, and after the foil sheet is separated from the die and the wires, the die and the wires connected to the respective die are separated from each other such that multiple packaged devices are formed substantially simultaneously.

15. A method of forming a plurality of integrated circuit packages, comprising the steps of:

providing a sheet of metal foil;

forming a layer of high temperature solder on a first side of the foil sheet via a screen printing process;

attaching first sides of a plurality of integrated circuit dies to the solder on the foil sheet, wherein the first side of each of the die includes a layer of metal thereon and a second, opposing side of each of the die includes a plurality of bonding pads;

performing a first reflow process for securing the plurality of integrated circuit dies to the metal foil;

electrically connecting the bonding pads to the foil sheet with a plurality of wires via a wirebonding process, wherein first ends of the wires are attached to the bonding pads and second ends of the wires are attached to the foil sheet;

encapsulating the integrated circuit dies, the electrical connections, and the first side of the foil sheet with a mold compound;

separating the foil sheet and the solder layer from the integrated circuit dies, second ends of the plurality of wires, and the mold compound via a second reflow process, wherein only

a portion of the solder layer is removed from the dice and the second ends of the plurality of wires; and

separating the encapsulated integrated circuit dies and the wires connected thereto from other ones of the encapsulated integrated circuit dies, thereby forming a plurality of packaged integrated circuits.

16. The method of packaging an integrated circuit according to claim 15, wherein squashed ball bonds are formed on the foil sheet, said ball bonds having a diameter of about 0.25 mm.

17. The method of forming a plurality of integrated circuit packages of claim 15, wherein the separating step comprises the step of saw singulating the encapsulated die from adjacent encapsulated dies.

18. A method of forming a multi-chip module, comprising the steps of:

providing a sheet of metal foil;

forming a layer of high temperature solder on a first side of the foil sheet via a screen printing process;

attaching first sides of at least two integrated circuit dies to the solder on the foil sheet, wherein the first side of each of the die includes a layer of metal thereon and a second, opposing side of each of the die includes a plurality of bonding pads;

performing a first reflow process for securing the at least two integrated circuit dies to the metal foil;

electrically connecting a first portion of the bonding pads of each of the at least two dies to the foil sheet with a plurality of first wires via a first wirebonding process,

wherein first ends of the first wires are attached to the bonding pads and second ends of the first wires are attached to the foil sheet;

electrically connecting the at least two dies to each other by connecting a second portion of the bonding pads of a first one of the die to a second portion of the bonding pads of a second one of the dies with a plurality of second wires via a second wirebonding process;

encapsulating the at least two integrated circuit dies, the electrical connections, and the first side of the foil sheet with a mold compound; and

separating the foil sheet and the solder layer from the at least two integrated circuit dies, second ends of the plurality of first wires, and the mold compound via a second reflow process, wherein only a portion of the solder layer is removed from the at least two dies and the second ends of the plurality of wires.

19. The method of forming a multi-chip module of claim 18, further comprising the steps of:

saw singulating the encapsulated die from adjacent encapsulated dice.

20. The method of forming a multi-chip module of claim 18, further comprising the steps of:

attaching a passive device to the solder on the foil sheet; and

electrically connecting the passive device to at least one of the at least two dies, and wherein the passive device is encapsulated with the mold compound.